REMARKS

The application has been amended to place the application in condition for allowance at the time of the next Official Action.

Claims 1, 3-8, 24 and 26-30 are pending in the application.

Claims 1, 4 and 30 are amended herewith. The amendment to claim 1 corrects a typographical error. The amendment to claim 4 clarifies the previously recited "thereof". The amendment to claim 30 presents claim 30 as in the amendment of September 9, 2005. Accordingly, the amendments only require a cursory review and do not raise any new issues requiring further search and/or consideration. Entry of these amendments is respectfully requested.

Claims 1, 3-8, 24 and 26-30 were rejected as unpatentable over SHEU et al. 6,694,208 in view of applicants' disclosed prior art. That rejection is respectfully traversed.

Claim 1 recites processing a wafer such that each of chip areas is produced as a semi-finished semiconductor device by forming a first metal wiring layer on each of the chip areas. Claim 1 also recites subjecting the wafer to a provisional yield-rate test in which it is examined whether each of the semi-finished semiconductor devices on the wafer is acceptable or unacceptable. Claim 1 further recites further processing to form a second metal wiring layer.

By way of example, as seen in Figure 1, reproduced below, wafer 10 is processed such that each of chip areas 12 is produced as a semi-finished semiconductor device by forming a first metal wiring layer 16 on each of the chip areas 12.

Figure 4, also reproduced below, shows the first metal wiring layer 16 formed on each of the chips 12. The probe (unnumbered and adjacent numeral 30) performs the provisional yield-rate test.

Fig. 1

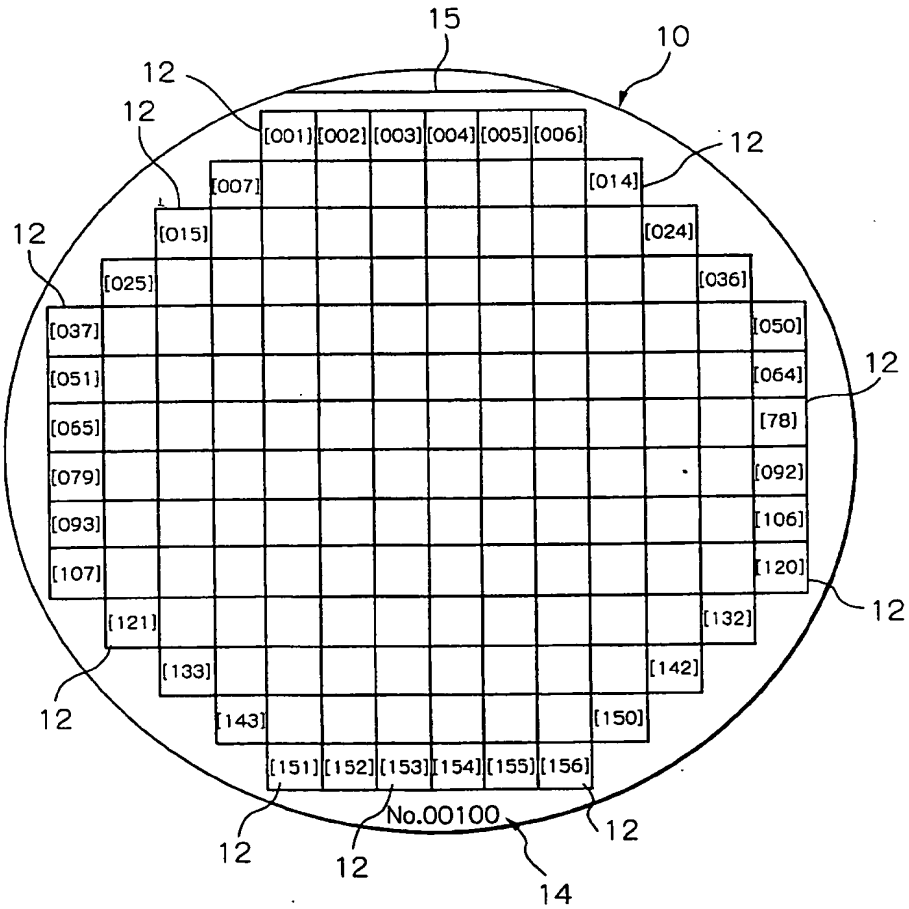


Fig. 4

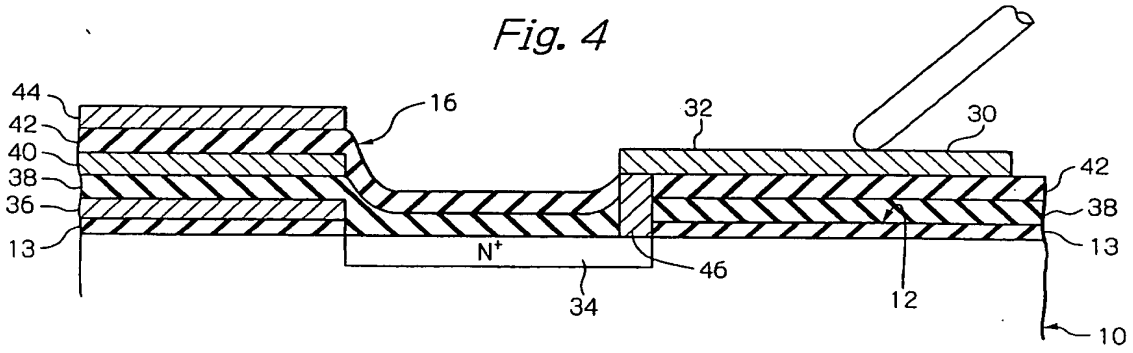
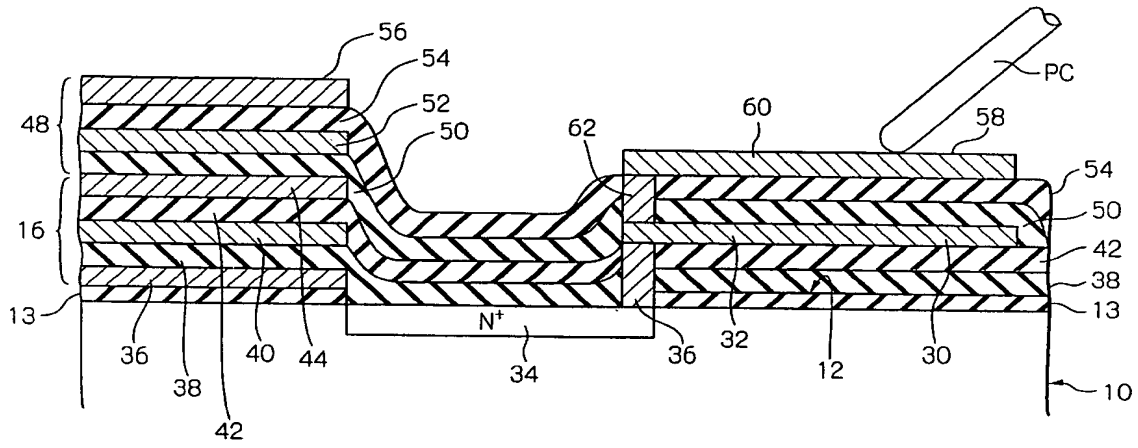


Figure 5, reproduced below, shows the finished wafer that has been further processed to form a second metal wiring layer 48 over the first metal wiring layer 16.

Fig. 5



The position set forth in the Official Action is that column 1, lines 20-25 and column 2, lines 57-65 of the SHEU reference disclose processing a wafer such that each of chip areas is produced as a semi-finished semiconductor device by forming a first metal wiring layer on each of the chip areas and subjecting the wafer to a provisional yield-rate test in which it is

examined whether each of the semi-finished semiconductor devices on the wafer is acceptable or unacceptable.

However, this characterization of SHEU is not supported by the disclosure of SHEU.

Column 1, lines 20-25 of SHEU disclose that to improve yield rate, test structure or test circuitry, is formed alongside the chips on the wafer to allow electrical tests to be conducted during and after manufacturing. (Emphasis added).

SHEU discloses performing a yield test on a test structure that is alongside a chip. SHEU does not disclose performing a provisional yield-rate test on a first wiring layer as recited.

Column 2, lines 57-65 of SHEU of SHEU define "soft defects" and how they may be corrected. This passage does not appear pertinent to how the yield-rate test is performed.

Applicants' disclosed prior art does not overcome the shortcomings of SHEU. Rather, as set forth on page 35, line 29 to page 36, line 4 in describing applicants' prior art Figure 17, a plurality of electrode pads, which the Official Action states are used as test pads, are formed simultaneously with the second metal wiring layer. Thus, test pads are not formed on and used to test a first wiring layer. Test pads are only on the second layer.

As SHEU uses a test pad alongside the chips and as applicants' disclosed prior art only has test pads on a second wiring layer. Performing a provisional yield-rate test on a first

wiring would not have been obvious to one having ordinary skill in the art.

Moreover, the processing in SHEU produces a finished product. Any further processing in SHEU is to produce new wafers based on information determined from earlier processing of a first set of wafers. There is no need to add a second wiring layer to the finished wafer of SHEU. Therefore, one of ordinary skill in the art would not have been motivated to further process the wafer of SHEU to form a second wiring layer, based on the results of the first wiring layer as recited in claim 1.

Neither the disclosed prior art nor SHEU disclose the formation of a second metal wiring layer on a first metal wiring layer after the wafer passes a provisional yield-rate test. Thus, their combination would not suggest these limitations.

Accordingly, for the reasons set forth above, claim 1 is believed patentable over the proposed combination of references.

Claims 3-8 depend from claim 1 and further define the invention and are also believed patentable over the cited prior art at least for depending from an allowable independent claim.

In addition, claim 4 recites that the basic wiring-arrangement section (the first wiring layer) has a plurality of electrode pads formed on an uppermost surface of the first wiring layer for carrying out a provisional yield-rate test.

As set forth above, page 35, line 29 through page 36, line 4 of the application as filed, disclose that electrode pads

58' are simultaneously formed with the uppermost metal circuit pattern layer 56' (second wiring layer). Applicants' disclosed prior art does not disclose a plurality of electrode pads formed on an uppermost surface of a first metal wiring layer.

SHEU does not disclose what is recited in claim 4. Accordingly, claim 4 is believed patentable regardless of the patentability of the claims from which it depends.

Independent claim 24 recites performing a provisional yield-rate test on a first test section of a first metal wiring layer. Claim 24 also recites forming a second metal wiring layer.

The analysis above regarding claim 1 is equally applicable to claim 24.

Claims 26-28 depend from claim 24 and further define the invention and are also believed patentable over the cited prior art at least for depending from an allowable independent claim.

Independent claim 29 recites a first metal wiring layer having a first test section and performing a provisional yield-rate test using the first test section. Claim 29 also recites further processing the wafer to form a second metal wiring layer.

As set forth above, column 1, lines 21-24 of SHEU disclose test circuitry formed alongside the chip, not on a test section of a first wiring layer.

In addition, the wafer of SHEU is a processed as a finished product, SHEU would not continue processing the wafer to form a second wiring layer as suggested in the Official Action.

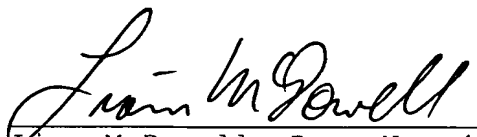
Independent claim 30 recites processing a wafer to form a first metal wiring layer and performing a provisional yield-rate test on the first metal wiring layer. Claim 30 also recites further processing the wafer to form a second metal wiring layer based on the results of the testing on the first metal wire layer. The analysis above regarding claim 1 is equally applicable to claim 30.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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